

WE CLAIM:

1. A digital blanking circuit, comprising:
an input connected to receive a digital input
signal,
a blanking interval circuit which triggers the
start of a blanking interval upon the occurrence of a
transition of said digital input signal, and
an output, said digital blanking circuit
arranged such that said output is prevented from re-
transitioning during said blanking interval and tracks
said digital input signal otherwise.

2. The digital blanking circuit of claim 1,
wherein said blanking interval circuit is arranged to
maintain said blanking interval for a first duration when
said digital input signal transitions from a low state to
a high state and to maintain said blanking interval for a
second duration when said digital input signal
transitions from a high state to a low state.

3. The digital blanking circuit of claim 1,
further comprising:

a rising edge latch which receives said digital
input signal and a first select signal at respective
inputs, said first select signal having first and second
states, said rising edge latch arranged to produce an
output which tracks said digital input signal when said
first select signal is in its first state and latches
said digital input signal upon the first occurrence of a
low-to-high transition of said digital input signal after
said first select signal transitions from its first state
to its second state,

a falling edge latch which receives said
digital input signal and a second select signal at

15 respective inputs, said second select signal having first
and second states, said falling edge latch arranged to
produce an output which tracks said digital input signal
when said second select signal is in its first state and
latches said digital input signal upon the first
20 occurrence of a high-to-low transition of said digital
input signal after said second select signal transitions
from its first state to its second state, and

 a two-to-one multiplexer which receives the
outputs of said rising and falling edge latches and a
25 third select signal at respective inputs, said third
select signal having first and second states, said
multiplexer arranged to transfer the output of said
rising edge latch to an output when said third select
signal is in its first state and to transfer the output
30 of said falling edge latch to said multiplexer output
when said third select signal is in its second state,
said multiplexer output being said digital blanking
circuit output,

 said blanking interval circuit connected to
35 receive said digital blanking circuit output at its input
and arranged to trigger a blanking interval having a
first duration upon the occurrence of a rising edge at
its input, to trigger a blanking interval having a second
duration upon the occurrence of a falling edge at its
40 input, and to provide said first, second and third select
signals such that said digital blanking circuit output is
prevented from re-transitioning during a blanking
interval.

4. The digital blanking circuit of claim 3,
wherein said blanking interval circuit is arranged such
that said first and second blanking interval durations
are equal.

5. The digital blanking circuit of claim 3, wherein said blanking interval circuit is arranged such that said first and second blanking interval durations are different.

6. The digital blanking circuit of claim 1, wherein said digital input signal propagates through a signal path to an output node at the end of said signal path, said signal path comprising said digital blanking circuit and at least one following stage which receives said digital blanking circuit's output, said blanking interval circuit connected to receive the signal at said output node at an adaptive input and arranged to terminate a currently-running blanking interval when the digital input signal transition which triggered the start of said currently-running blanking interval has propagated through said signal path to said output node and said adaptive input, the duration of said blanking interval thereby automatically adjusted to be equal to the propagation delay of a signal through said signal path.

7. The digital blanking circuit of claim 6, wherein said blanking interval circuit is arranged to terminate a currently-running blanking interval only upon the occurrence of a rising edge at said adaptive input.

8. The digital blanking circuit of claim 6, wherein said blanking interval circuit is arranged to terminate a currently-running blanking interval only upon the occurrence of a falling edge at said adaptive input.

9. A digital blanking circuit, comprising:
a rising edge latch which receives a digital input signal and a first select signal at respective

inputs, said first select signal having first and second
5 states, said rising edge latch arranged to produce an
output which tracks said digital input signal when said
first select signal is in its first state and latches
said digital input signal upon the first occurrence of a
low-to-high transition of said digital output signal
10 after said first select signal transitions from its first
state to its second state,

a falling edge latch which receives said
digital input signal and a second select signal at
respective inputs, said second select signal having first
15 and second states, said falling edge latch arranged to
produce an output which tracks said digital input signal
when said second select signal is in its first state and
latches said digital input signal upon the first
occurrence of a high-to-low transition of said digital
20 output signal after said second select signal transitions
from its first state to its second state, and

a two-to-one multiplexer which receives the
outputs of said rising and falling edge latches and a
third select signal at respective inputs, said third
25 select signal having first and second states, said
multiplexer arranged to transfer the output of said
rising edge latch to an output when said third select
signal is in its first state and to transfer the output
of said falling edge latch to said multiplexer output
30 when said third select signal is in its second state,
said multiplexer output being said digital blanking
circuit output,

a blanking interval circuit having an input
connected to receive said digital blanking circuit output
35 and arranged to trigger a blanking interval having a
first duration upon the occurrence of a rising edge at
its input, to trigger a blanking interval having a second
duration upon the occurrence of a falling edge at its

input, and to provide said first, second and third select
40 signals such that said digital blanking circuit output is
prevented from re-transitioning during a blanking
interval.

10. The digital blanking circuit of claim 9,
wherein said blanking interval circuit is arranged such
that said first and second blanking interval durations
are different.

11. The digital blanking circuit of claim 9,
wherein said blanking interval circuit is arranged such
that said first and second blanking interval durations
are equal.

12. The digital blanking circuit of claim 9,
wherein said blanking interval circuit is arranged to,
upon the expiration of each of said blanking intervals
triggered by a falling edge, provide said first, second,
5 and third select signals such that said rising edge latch
is set to latch, said falling edge latch is set to track,
and said multiplexer is set to transfer said rising edge
latch's output to said digital blanking circuit output,
and upon the expiration of each of said blanking
10 intervals triggered by a rising edge, to provide said
first, second, and third select signals such that said
falling edge latch is set to latch, said rising edge
latch is set to track, and said multiplexer is set to
transfer said falling edge latch's output to said digital
15 blanking circuit output.

13. The digital blanking circuit of claim 9,
wherein said digital input signal propagates through a
signal path to an output node at the end of said signal
path, said signal path comprising said digital blanking

5 circuit and at least one following stage which receives
said digital blanking circuit's output, said blanking
interval circuit connected to receive the signal at said
output node at an adaptive input and arranged to
10 terminate a currently-running blanking interval when the
digital input signal transition which triggered the start
of said currently-running blanking interval propagates
through said signal path to said output node and said
adaptive input, the duration of said blanking interval
15 thereby automatically adjusted to be equal to the
propagation delay of a signal through said signal path.

14. The digital blanking circuit of claim 13,
wherein said blanking interval circuit further includes a
timer which begins timing at the start of a blanking
interval and times out at the expiration of a
5 predetermined time period, said timer arranged to
terminate said blanking interval if said blanking
interval is not already terminated via said adaptive
input.

15. The digital blanking circuit of claim 13,
wherein said blanking interval circuit further includes a
timer connected in series with said adaptive input and
arranged to delay the termination of said blanking
5 interval via said adaptive input such that said blanking
interval is extended to cover any noise-induced
transitions at said output node.

16. The digital blanking circuit of claim 13,
wherein said blanking interval circuit is arranged to
terminate a blanking interval only upon the occurrence of
a rising edge at said adaptive input.

17. The digital blanking circuit of claim 13,

wherein said blanking interval circuit is arranged to terminate a blanking interval only upon the occurrence of a falling edge at said adaptive input.

18. The digital blanking circuit of claim 9, wherein said rising edge latch comprises first and second two-input NOR gates, said first NOR gate connected to receive said digital input signal at one input and the output of said second NOR gate at its other output, said
5 second NOR gate receiving the output of said first NOR gate at one input and said first select signal at its other input, the output of said first NOR gate being the output of said rising edge latch.

19. The digital blanking circuit of claim 9, wherein said falling edge latch comprises first and second two-input NAND gates, said first NAND gate connected to receive said digital input signal at one input and the output of said second NAND gate at its
5 other output, said second NAND gate receiving the output of said first NAND gate at one input and said second select signal at its other input, the output of said first NAND gate being the output of said falling edge
10 latch.

20. The digital blanking circuit of claim 9, wherein said rising edge latch comprises first and second two-input NOR gates, said first NOR gate connected to receive said digital input signal at one input and the
5 output of said second NOR gate at its other output, said second NOR gate receiving the output of said first NOR gate at one input and said first select signal at its other input, the output of said first NOR gate being the output of said rising edge latch, said falling edge latch
10 comprises first and second two-input NAND gates, said

first NAND gate connected to receive said digital input signal at one input and the output of said second NAND gate at its other output, said second NAND gate receiving the output of said first NAND gate at one input and said
 15 second select signal at its other input, the output of said first NAND gate being the output of said falling edge latch, further comprising an inverter connected to the output of said multiplexer, the output of said inverter being the output of said digital blanking
 20 circuit.

21. A system which includes a digital blanking circuit, comprising:

a signal source which produces a digital input signal,

5 a following circuit which receives a signal representing said digital input signal at an input and which produces an output that varies with said received signal, and

a digital blanking circuit, comprising:

10 a rising edge latch which receives said digital input signal and a first select signal at respective inputs, said first select signal having first and second states, said rising edge latch arranged to produce an output that tracks said digital input signal when said first select signal is in its first state and
 15 latches said digital input signal upon the first occurrence of a rising edge after said first select signal transitions from its first state to its second state,

20 a falling edge latch which receives said digital input signal and a second select signal at respective inputs, said second select signal having first and second states, said falling edge latch arranged to produce an output that tracks said digital input signal

25 when said second select signal is in its first state and
latches said digital input signal upon the first
occurrence of a falling edge after said second select
signal transitions from its first state to its second
state, and

30 a two-to-one multiplexer which receives
the outputs of said rising and falling edge latches and a
third select signal at respective inputs, said third
select signal having first and second states, said
multiplexer arranged to transfer the output of said
35 rising edge latch to an output when said third select
signal is in its first state and to transfer the output
of said falling edge latch to said output when said third
select signal is in its second state, said multiplexer
output being said digital blanking circuit output,

40 a blanking interval circuit having an
input connected to receive the output of said following
circuit and arranged to trigger a blanking interval
having a first duration upon the occurrence of a rising
edge at its input, to trigger a blanking interval having
45 a second duration upon the occurrence of a falling edge
at its input, and to provide said first, second and third
select signals such that said digital blanking circuit
output is prevented from re-transitioning during a
blanking interval, said digital blanking circuit thereby
50 preventing said following circuit output from re-
transitioning before the previous transition of said
digital input signal has propagated through said system
to said following circuit output.